Simulation and Design of an HDP-CVD Process for Planar Spacer Applications for Future DRAM Cell Concepts

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Abstract

High Density Plasma Chemical Vapor Deposition is a well known process for gap-fill applications. This paper describes the usage of High Density Plasma Chemical Vapor Deposition to generate a buried isolation layer (Planar Spacer). A study to meet Planar Spacer requirements is presented based on simulations on reactor and feature scale. It explains variations from wafer center towards the edge in within-trench fill height uniformity, sidewall coverage and hat height. Plasma density variations across the wafer surface and subsequently deviations of incoming ions off the normal direction were found as the main contributor. Simulation results could be confirmed by several experiments. Based on this results a new type of High Density Plasma Chemical Vapor Deposition process was designed to achieve homogenous within trench fill heights and pattern across the wafer and is therefore suitable for Planar Spacer applications.

INTRODUCTION

With the shrinkage of the technology node down to 50nm, new DRAM cell concepts are under development. Such a new DRAM cell concept is the Vertical Transistor Cell design [1]. Within this concept a new type of layer is needed to isolate the capacitor from the active transistor area. This Planar Spacer like buried isolation is called Top Trench Oxide (see Figure 1).

High Density Plasma - Chemical Vapor Deposition (HDP-CVD) processes are widely used in Semiconductor Industry for gap-fill applications like Shallow Trench Isolation (STI) and Inter Metal Dielectric (IMD) since 0.25µm technology node. Beside these gap-fill applications, HDP-CVD can also be used to form Planar Spacers within trench structures by using it as a partial fill, utilizing the HDP-CVD characteristic of different bottom versus sidewall oxide growth rates. Since thickness on a trench bottom is always greater then on vertical sidewalls after the HDP deposition, after a subsequent isotropic wet etch step, oxide remains in the trench bottom and serves as the isolation.

Specifications for that new Planar Spacer application like high film quality, flat within trench surface topology, uniform within trench thickness between wafer center and edge are different to that of gap-filling processes and require therefore new process development. A comparison of the requirements is provided in Table 1.

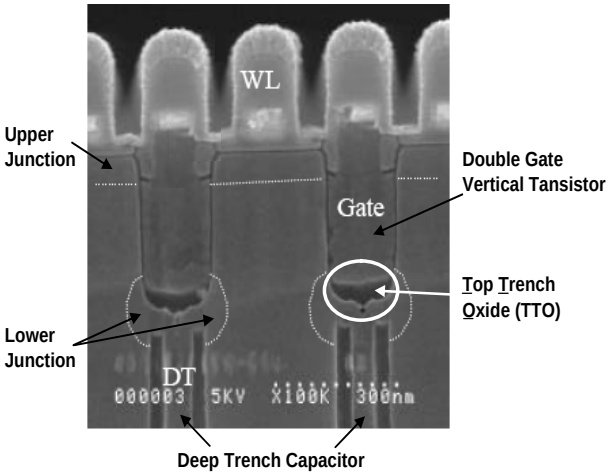

Figure 1. SEM micrograph of a Vertical Transistor Cell with targeted TTO [1].

Table 1. Comparison of conventional gap-fill (STI) versus new Planar Spacer applications.

Shallow Trench Isolation @ 90nm GR		Planar Spacer @ 90nm GR	
Line-Space	90 nm	Hole	160x90 nm
Depth	~400 nm	Depth	~400 nm
AR	~ 4.5:1	AR	~ 4.5:1
Film Thickness	> 500 nm	Film Thickness	100 nm
Requirements: 1. Complete gap-fill, no voids 2. Good WIW film uniformity 3. No damage to active regions		Requirements: 1. Partial Fill (Bottom film thickness greater than sidewall film thickness) 2. Thickness at trench bottom must be very uniform across the wafer 3. Within trench profile of deposited material must be flat	

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PROBLEM DESCRIPTION

In order to fill trenches with a high Aspect Ratio (AR), HDP-CVD process utilizes high density plasma and low pressures. Such a process is capable of fully gap-filling trenches with dimensions as described in Table 1 left side and as shown in Figure 2. However, this process regime yields in tilted within-trench profiles, which disqualify them from meeting Planar Spacer stringent requirements, as seen in Figure 3.

The purpose of this study is to identify which key parameters impact within-trench profile through simulation, verify simulation results with experiments on structured wafers and find suitable process condition to meet Planar Spacer requirements.

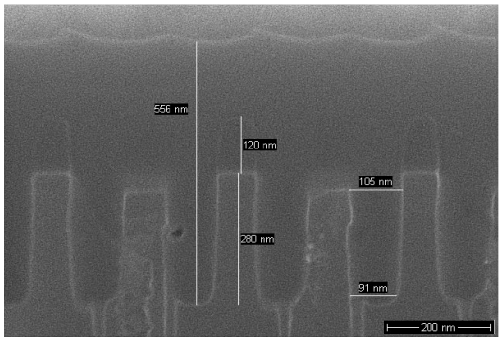

Figure 2. SEM micrograph of complete filled 90nm DRAM IT structures from wafer-edge. The used HDP process was optimized for gap-fill.

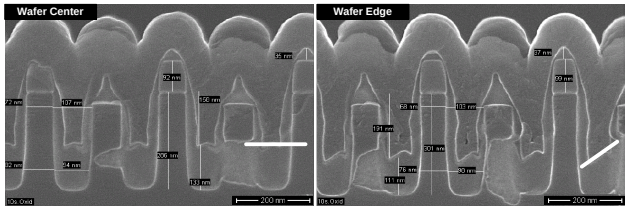

Figure 3. SEM micrographs of partial filled trenches at wafer-center and edge for gap-fill optimized process. Polysilicon added for clarity.

SIMULATION

Physical Model of the Within-Trench Profile of an HDP-CVD Deposition

The underlying physical model to understand the described problem is explained in the following section. Figure 4 is used to illustrate this model. The plasma confining geometry as well as the location and design of power coupling is deciding on the uniformity of the plasma density across the wafer. The electrical field in the plasma reactor follows mainly the plasma density distribution. Altogether, the electrical field is not always exactly normal to the wafer. e.g. for a plasma centered in the middle of the reactor, the horizontal component of the electrical field increases towards the wafer's edge, which accelerates the incident ions non-perpendicular with respect to the wafer's surface.

Figure 4 shows an ion trajectory. After the last collision of the ion with the neutral background gas the ion is accelerated freely to the wafer surface. The relevant quantity here is the deflection angle α of the ion relative to the surface normal. This angle was derived from energy conservation considerations and is a function of the potential variations ΔU over the wafer.

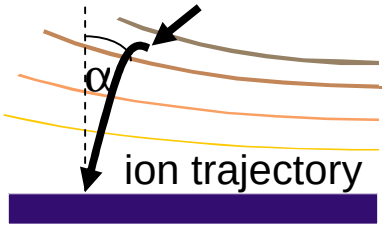

Figure 4. Schematics of an ion trajectory at the wafer edge.

Reactor Scale Plasma Simulation

The potential variation ΔU over the wafer is calculated from our custom reactor scale plasma simulation tool. Therefore, a typical ICP plasma reactor was simulated and two limiting cases of different power coupling were investigated: (1) edge (or side) coils powered, and (2) center (or top) coils powered.

Results for the electrical potential within the reactor are in Figure 5 for the two scenarios. For the edge coils powered, the distribution of the electrical potential (Figure 5 right side) is torus -like with maximum underneath the outer coil. In contrast, Figure 5 -left side- represents the electrical potential for the center coil powered case. Here, the maximum in potential is located nearly at the middle of the reactor. The uniform electrical fields (vectors) highlight the maxima for both scenarios.

Deflection Angle of Ions on Wafer Surface

After extracting ΔU from the reactor scale plasma simulation the deflection angle α can be calculated. Figure 6 plots this incidence angle over radius. For the torus-like potential distribution of the edge powered coils the maximum of deflection angle is within the wafer nearly at half radius.

The center coil powering scenario yields in a nearly linearly increase of deflection angle over radius. Thus, by varying the power coupling geometrically it is possible to steer and optimize the deflection of ions over the wafer radius.

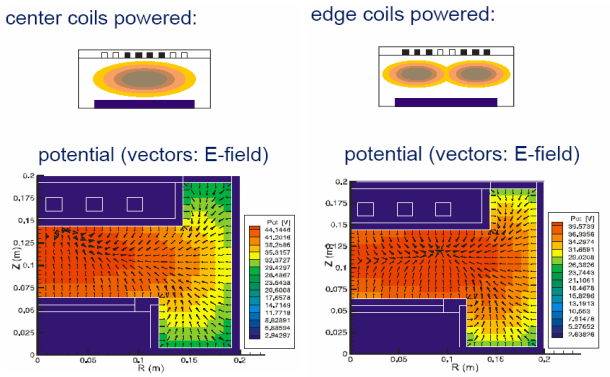

Figure 5. Electrical potential in Volts (contours) and electrical field (vectors) for edge coils vs. center coils powered.

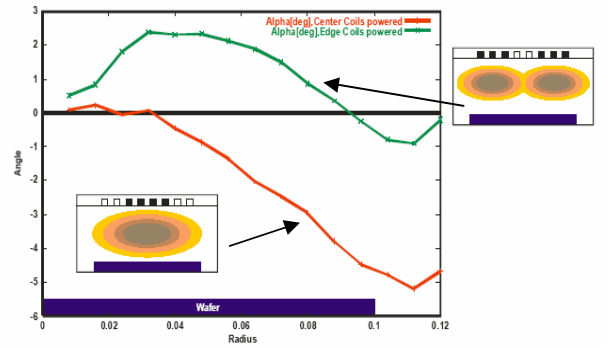

Figure 6. Deflection angle of ions over wafer for center and edge powered coil configuration.

Feature Scale Simulations

Using the ion deflection angle from the reactor scale plasma simulation, the temporal evolution of line-space structures was studied using our custom feature scale simulator Topsi3D. Details of this simulator have already been published elsewhere [2]. To summarize, Topsi3D calculates particle transport via Monte-Carlo and couples it to a chemistry solver capable of arbitrary surface reactions. The local deposition or etch rates are used to propagate the surface using the level set method [3]. The updated front is then used to re-sample gas and ion fluxes. This procedure is repeated until the specified oxide thickness is reached.

The HDP-CVD chemistry model used in this work was inspired by a reactor scale model by Meeks et al. [4] which has been extended to the feature scale. Details of this model can be found in [5]. Basically SiO_2 growth is via ion-enhanced deposition of neutral precursors. After a neutral molecule binds on a reactive site, this site is passivated until re-activation by an energetic ion takes place. Other surface reactions in the model include ion-milling (→ sputter edges at high energy), thermal activation (→ conformal deposition), and ion reflection (→ overhangs at opposite wall). For all reactions, a rate and, in the case of ionic reactions, an energy and angle dependent yield was taken from literature [6] or calibrated to data. Using:

- this chemistry model,
- the potential variation ΔU from the reactor scale simulation and
- the calculated ion deflection angle

an HDP-CVD process with a center coil powered configuration was simulated. This configuration was chosen to link the plasma density profile with the deposition profile. The simulation result versus SEM images from a center coil powered HDP-CVD process on comparable wafer structures (line-space) are shown in Figure 7. Note that sputtering is negligible for the low bias power used for the above experiments. The simulation results can be summarized as following:

- Simulation reproduces very well that the deposited film within the trench is more tilted at the wafer edge compared to wafer center. Specifically, both the tilted bottom and the slight shift in top hat position are visible in the simulation results.
- The results of the Reactor Scale Plasma Simulation strongly recommend the theory that the within-trench tilted profile is caused by a radial potential drop in the plasma pre-sheath.
- The extensive matching of simulated and real growth characteristic of an HDP-CVD film indicates that HDP-CVD SiO_2 growth can be described as an ion-enhanced deposition of neutral precursors.

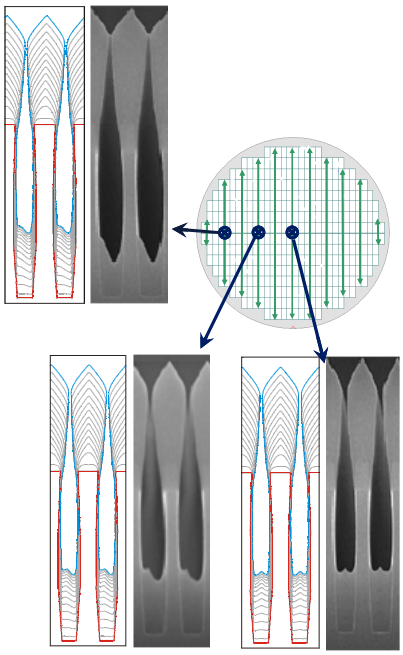

Figure 7. Simulation and SEM micrographs of line-space structures taken at the indicated radii. HDP-CVD process was done in a center coil powered regime.

EXPERIMENTAL

A conventional 200mm HDP-CVD reactor from Applied Materials Inc. was used. This HDP-CVD reactor is designed with two independent coils to apply RF to the chamber - a top coil, which is located right above the wafer, and a side coil, which mounted to the side of the reactor and encloses the wafer (Figure 8). Furthermore the gas injection system is also separated into a side injection and a top injection system

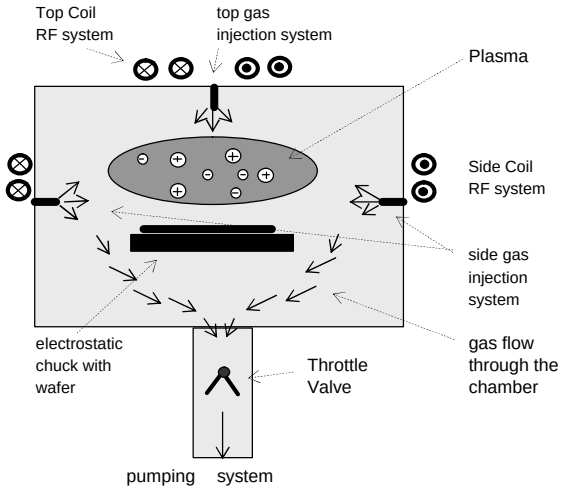

Figure 8. Sketch of the used HDP-CVD reactor.

Two types of experiments were performed on this HDP-CVD reactor to check the modelling for accuracy. Within the first set of experiments the plasma density was measured for positions at the center and the edge of the plasma. Various RF set points were applied to the chamber during this measurement. The plasma density was measured by using a Langmuir Probe.

The second set of experiments was covering a large number of HDP deposition tests by using the described HDP reactor. A SiO_2 film was deposited on blanket and structured wafers. For cost reasons the structures utilized were Isolation Trenches on 90nm ground-rule. Those Isolation Trenches were filled partially to measure the thickness of the deposited SiO_2 within these trenches. The test wafers were cleaved on two different positions – at the wafer center and at the extreme edge of the wafer (Figure 9).

These two different cleaving positions were used to compare the bottom-up SiO_2 film, by a) its thickness and b) the flatness of its deposition profile.

Within this second set of experiments a standard HDP-CVD process was used, applying conventional process gases like SiH_4, O_2, and inerts. To ensure a comparable process performance through all tests, the Deposition-Sputter-Ratio was tuned to be equal for every single test. Deposition-Sputter-Ratio is one of the key parameter for an HDP-CVD process, which is used to characterize the SiO_2 deposition and the physical sputtering on blanket wafers.

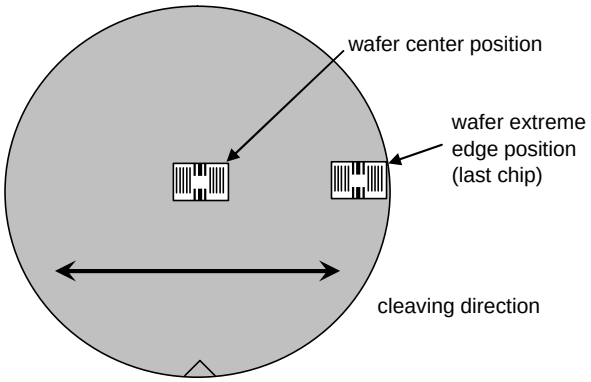

Figure 9. Cleaving positions on the wafer after performing HDP deposition tests.

RESULTS

Plasma Density Measurement

The Saturation Current (I_{sat}) of the Langmuir apparatus was used to monitor the plasma density at two different spots – one above the wafer center and one above the wafer edge. The experiments were split into two portions:

- variation of the applied RF power with the top coil to the half and the maximum RF generator output, keeping the applied RF power from the side coil at zero and
- variation of the applied RF power with the side coil to the half and the maximum RF generator output, keeping the applied RF power from the top coil at zero.

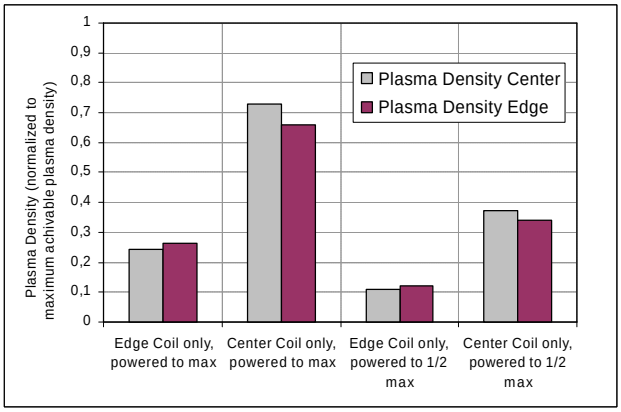

Figure 10. Plasma density measurement (Langmuir Probe, Helium Plasma) at the center and the edge of the reactor, normalized to the maximum achievable plasma density.

The experimental setup was designed to review the results of Figure 5, which shows the simulated distribution of the electrical potential across a reactor for a center- or edge-powered plasma.

The Langmuir probe measurements (Figure 10) show that:

- RF, applied to the top coil, results in an approximately 3 times higher Plasma Density than the same RF, applied to the side coil,
- operating the reactor with a side coil results in an almost homogenous plasma density distribution, whereas the top coil is driving the plasma to be more non-uniform across the wafer.

Just as the simulation results, the Langmuir data are also pointing to a potential Planar-Spacer process with a side coil powered plasma, using a lower top coil RF value for fine-tuning.

HDP Deposition Tests on Structured Wafers

To assess the Planar-Spacer non-uniformity across the wafer, this parameter is defined as

$$NU_{Planar\text{-}Spacer} = [(BU_{center} - BU_{edge}) / (2 * Mean_{OpenArea})] * 100$$

with

BU = *Bottom-Up Thickness within Trench*
$Mean_{OpenArea}$ = *Average Thicknesses in Open Areas at Wafer-Center and Wafer-Edge*

For example, the $NU_{Planar\text{-}Spacer}$ for the data as presented within Figure 3 would be at 8.2%.
Some of the experimental results are listed in Table 2. Either hardware or process changes were tested and assessed by using standard types of HDP-CVD processes.
Two experimental setups out of the complete set of tests were showing significant improvements of the $NU_{Planar\text{-}Spacer}$ and the flatness of deposition profiles within a trench.

Table 2: An extract from the list of the performed experiments on structured wafers and its results.

Test Details	Rank	NU [%]	Profile of the bottom deposition within a trench
Baseline of the standard process	8	11.7	tilted
Second process with different chemistry	6	8.8	tilted
Gas injectors with a larger orifice	7	9.0	tilted
Gas injectors introducing process gases towards the top of the reactor	5	6.2	tilted
Side RF coil was switched off	6	8.8	tilted
Oxygen was also introduced from top injectors	4	5.9	tilted
Top RF coil inner diameter was increased	3	2.1	tilted
High inert gas flow from the top injection was removed, a throttle valve was moved to a closed position to maintain comparable process pressure	2	0.3	tilted
Low top source RF	1	2.2	flat

Turning off the Top Coil RF

Turning off the RF power from the top coil reduced the $NU_{Planar\text{-}Spacer}$ to 2.2%, but didn't eliminate it down to zero. The deposition within a trench was changed to a totally flat profile on the wafer edge area.

Modified Gas-Flow

Within that experiment:

- all gases were introduced only from the side-injectors and the total gas flow was reduced to a value of less than 150sccm and
- the Throttle Valve was moved to an almost closed position to maintain a typical HDP-CVD process pressure (1-10mTorr).

This experiment resulted in a decreased $NU_{Planar\text{-}Spacer}$ down to 0.3%. But although the required low $NU_{Planar\text{-}Spacer}$ could be achieved, the deposition within the trench still shows a tilted profile at the wafer edge area.

DISCUSSION

The simulation of an HDP-CVD process concluded a large difference in plasma density to create a significant gradient of the Deflection Angle α and of the E-field over the radius of the wafer.
The experimental data confirmed this large plasma density gradient to be the main driver for the tilted deposition at the bottom of a trench at the wafer edge. Simulated and experimental data matches.
As experimental data show, there are more factors than RF variations influencing the $NU_{Planar\text{-}Spacer}$ − such as process pressure, gas flow pattern etc. These factors are directly linked to the plasma density distribution across the wafer and do not oppose the presented simulation.
The matching of the simulation results and experimental data confirmed the validity of using the presented model to simulate an HDP-CVD process. So, HDP-CVD can be described as an ion-enhanced deposition of neutral precursors. The energetic activation of a wafer surface by the ion flux of the plasma is an essential requirement to deposit SiO_2 via HDP-CVD. And the uniformity of the ion-enhanced activation of the wafer surface (and thus the $NU_{Planar\text{-}Spacer}$) is driven by plasma density gradients and with it by the Deflection Angle of ions.

Based on the results, an HDP-CVD process for a Planar Spacer application is characterized by two components:

- RF which is applied to the side coil is significantly higher then RF which is applied to top coil.
- The plasma carrier gas must flow through the side injection at a low flow value, in addition with closing the Throttle Valve for a better carrier gas distribution across the wafer.

Furthermore the ratio of SiO_2 deposition at trench bottom versus trench sidewall itself, important for the process integration, is adjustable by the overall plasma density.
The flexibility of the utilized reactor enables to design an HDP-CVD process which is applicable for Planar Spacer applications. Only limitation was given by the maximum of achievable RF side coil power.

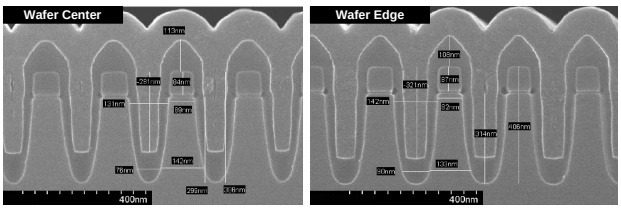

Figure 11. SEM micrographs of partial filled trenches at wafer-center and edge. The used HDP-CVD process was optimized towards a Planar Spacer application. No tilt and almost the same bottom-up SiO_2 thickness across the wafer is achieved. Polysilicon added for clarity.

Figure 11 is an example of a Planar Spacer process applied to a trench structure, satisfying all three requirements:

- The deposited SiO_2 thickness within a trench is much thicker at the bottom than at the side-walls of the trench (ratio 3:1).
- The deposited SiO_2 thickness at the bottom of the trench is very uniform across the wafer.
- The profile of deposited SiO_2 at the bottom of the trench is flat.

REFERENCES

[1] R. Weis et al. *"A highly cost efficient 8F2 DRAM Cell with Double Gate Vertical Transistor Device for 100nm and beyond"*, IEDM, 2001

[2] W. Jacobs et al., *"A Feature Scale Model for Trench Capacitor Etch Rate and Profile"*, Digest of the International Electron Devices Meeting 2002, p.891-4

[3] J.A. Sethian, *"Level set methods and fast marching methods"*, Cambridge Monographs on Applied and Computational Mathematics, ISBN 0-521-64204-3

[4] E. Meeks et al., *"Modeling of SiO_2 deposition in high density plasma reactors and comparisons of model predictions with experimental measurements"*, J. Vac. Sci. Technol. A, vol 16, No. 2, pp. 544-563, 1998

[5] A. Kersch, G. Schulze-Icking, *"Recent Advances in feature Scale Simulation"*, Digest of the International Electron Devices Meeting 2000

[6] C. F. Abrams et al., *"Energetic ion bombardment of SiO_2 surfaces: Molecular dynamics simulations"*, J. Vac. Sci. Technol., vol 16, No 5, pp 3006-3019, 1998

BIOGRAPHY

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